REMARKS

Favorable reconsideration of this application in light of the following remarks is respectfully requested.

Claims 1-12 are pending within this application. No claims are amended herein. No claims have been allowed.

Claim Rejections - 35 U.S.C. § 102

The Examiner has rejected claims 1-2, 7-8 and 12 under 35 U.S.C. § 102(b) as being anticipated by applicant's admitted prior art.

In response, applicant respectfully disagrees within the Examiner's reading of applicant's admitted prior art insofar as the Examiner within the paragraph bridging pages 2-3 of the office action mailed on 24 September 2002 characterizes applicant's thermal oxidizing process step 24 in applicant's Fig. 5 as a supplemental thermal annealing process step in accord with applicant's claim 1, last clause and applicant's claim 8, last clause.

Rather, applicant's thermal oxidizing process step 24 in applicant's Fig. 5 is employed for forming applicant's third gate oxide layer 22 upon applicant's active region 11c of applicant's three times thermally oxidized semiconductor substrate 10"' (page 19, second full paragraph), and is thus not a supplemental thermal annealing process step but rather a non-supplemental thermal oxidizing process step which is employed for forming a specific gate dielectric layer of a specific thickness upon a specific active region of applicant's semiconductor

substrate Within applicant's admitted prior art as illustrated in Fig. 1 to Fig. 5 and as cited by the Examiner, applicant's thermal oxidizing process steps 16, 20 and 24 are employed for forming applicant's corresponding gate dielectric layers 14a, 18a and 22 upon applicant's corresponding active regions 11a, 11b and 11c of applicant's three times thermally oxidized semiconductor substrate 10"', and thus there is no supplemental thermal annealing process step employed within applicant's admitted prior art.

Thus, since each and every limitation within applicant's invention as disclosed and claimed within claim 1 and claim 8 is not disclosed within applicant's admitted prior art, in particular with respect to a supplemental thermal annealing process step for thermally annealing a semiconductor substrate to compensate for forming thereupon a plurality of gate dielectric layers having less than a corresponding maximum numbered plurality of differing thicknesses formed employing less than a corresponding maximum numbered plurality of thermal oxidation process steps, applicant asserts that claim 1 and claim 8 may not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by applicant's admitted prior art.

Since all remaining claims within this rejection are dependent upon claim 1 or claim 8 and carry all of the limitations of claim 1 or claim 8, applicant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by applicant's admitted prior art.

Claim Rejections -- 35 U.S.C. § 103

The Examiner has rejected claims 3-6 and 9-11 under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art.

While not precluding the existence of independent patentable distinctions between: (1) applicant's admitted prior art; and (2) that which is claimed within claims 3-6 and 9-11, applicant predicates patentability of applicant's claims 3-6 and 9-11 upon their dependence upon applicant's claim 1 or claim 8.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of applicant's claims 3-6 and 9-11 under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art be withdrawn.

Other Considerations

Applicant acknowledges the prior art of record cited by the Examiner, but not employed in rejecting applicant's claims to applicant's invention, including: (1) Su et al. (U.S. Patent No. 5,576,573); (2) Gardner et al. (U.S. Patent No. 6,054,374); (3) Jenq (U.S. Patent No. 6,303,521); (4) Pearce et al. (U.S. Patent No. 6,358,865); and (5) Mukhopadhyay et al. (U.S. Patent No. 6,399,488), as generally pertinent to applicant's invention.

No fee is due as a result of this response.

SUMMARY

Applicant's invention as disclosed and claimed within claim 1 and claim 8 is directed towards a method for fabricating a semiconductor substrate to form thereupon a plurality of gate dielectric layers having less than a corresponding maximum numbered plurality of differing thicknesses formed employing less than a corresponding maximum numbered plurality of thermal oxidation process steps. The method employs a supplemental thermal annealing process step, which is absent from applicant's admitted prior art, to compensate for the less than corresponding maximum numbered plurality of thermal oxidation process steps.

CONCLUSION

On the basis of the above remarks, reconsideration of this application, and its early allowance, are respectfully requested.

Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,

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APPENDIX

COMPLETE COPY OF THE CLAIMS

(MARKED-UP WITH CURRENT REVISIONS)

1. A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having a maximum numbered plurality of differing thicknesses formed employing a corresponding maximum numbered plurality of thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate to compensate for forming thereupon the plurality of gate dielectric layers having less than the corresponding maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps.

2. The method of claim 1 wherein the maximum numbered plurality is at least three.

3. The method of claim 1 wherein the maximum numbered plurality is greater than three.

4. The method of claim 1 wherein the plurality of differing thicknesses encompass a range including a low thickness of from about 10 to about 40 angstroms and a high thickness of from about 50 to about 200 angstroms.

5. The method of claim 1 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

6. The method of claim 1 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

7. The method of claim 1 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.

8. A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having three differing thicknesses formed employing three thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the three differing thicknesses formed employing less than the three thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate to compensate for forming thereupon the plurality of gate dielectric layers having the less than three differing thicknesses formed employing the less than three thermal oxidation process steps.

9. The method of claim 8 wherein the plurality of differing thicknesses encompass a range including a low thickness of from about 10 to about 40 angstroms and a high thickness of from about 50 to about 200 angstroms.

10. The method of claim 8 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

11. The method of claim 8 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

12. The method of claim 8 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.